CMOS Low-Noise Amplifier for 2.4-GHz Wireless Receivers

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Abstract—This paper describes a 2.4GHz low noise amplifier (LNA) intended for use in receiver system. The design has been done in 180nm technology using CMOS. The proposed LNA uses inductive degeneration technique. This amplifier provides a forward gain of 15.72dB with a low noise figure of .307dB while drawing 6.5mW from 1.8V supply voltage. The LNA uses a transformer as load. This paper presents a detailed analysis of the used design methodology and measured results.

Keywords—LNA; low-noise amplifier(LNA); noise figure; gain; IIP3; NC; RF.

I. INTRODUCTION

Radio frequency (RF) is the electromagnetic wave frequency that lie in the range from around 3KHz to 300GHz. Signal coming from antenna is RF signal. Radio Frequency circuits are used into everything that transmits and receives a radio wave, which includes mobile phones, radios, Wi-Fi, and two-way radios. Wireless local area networks (WLAN’s) in the 2.4-GHz range have rapidly emerged in the consumer market [1]. The advantage of using CMOS for RF circuit is ease of integration of digital section. This cause to whole system on chip. CMOS has become a competitive technology for radio transceiver implementation of various wireless communication systems due to technology scaling, higher level of integrability, lower cost, etc. [2].

Low noise amplifier (LNA) is used in receiver at the first stage. Typically, the first block of a receiver is LNA [3]. It affects the performance of receiver. The overall performance of the receiver system depends on the LNA noise figure and gain. The design of LNA faces several challenges such as linearity, low noise figure (NF), impedance matching, sufficient gain and low power consumption because it should achieve high gain to suppress the noise. We try to design LNA such that it should provide a minimum noise figure while providing sufficient linearity with gain, IIP3 and a stable 50Ω input impedance. Good input matching is critical when a preselect filter precedes the LNA. Application of LNA is to amplification before the mixer.

Active mixers provide active gain. But they are consuming some DC power, because of this LNA gain can be relaxed. But power consumption by LNA needs to be low to compensate the power consumption of active mixer. LNA should have good NF. Communication systems implementation with the standard, which includes low power and low data rate. So, the design of LNA is aimed at lower power consumption A heterodyne receiver, diagrammed in fig1. Heterodyne receiver is used in various applications such as broadcast reception, mobile radio application and two way radio communications. It include a low-Noise Amplifier followed by image rejected filter that is used to remove signals on the image frequency. Analog to Digital converter followed by digital signal processing aimed at recovering the information data.

This paper include the design and implementation of Low Noise Amplifier in a 180nm technology. The paper is organised in four section. In section I, introduction of design are summarized. In section II, the proposed circuit is analyzed, and design specification are shown in table I. In section III, simulation results, and comparison of the design are analysed in table II. Section IV shows a conclusion of this work.

II. ARCHITECTURE AND CIRCUIT DESIGN

The way of input matching is shown in figure 2, which is classified into four architectures [4]. Resistance match, feedback structure, common gate structure and inductive degeneration are shown below. In Resistance Match Structure (a), we are going to make resistance equal to Zin for power matching, because of this input voltage cut by half before amplification and adding noise due to resistance. Noise Figure for this structure is given by Eq. (1).

\[
NF = 2 + \frac{NF_{1}}{a_{gmds}}
\]  

(1)

So here NF always greater than 3dB.

Fig. 2. Heterodyne Receiver
In Feedback Match Structure (b), thermal noise is adding due to feedback resistance and Noise Figure is still greater than the resistance match structure. In Common Gate Structure Noise Figure depend on device parameters $\gamma$ and $\alpha$, we ignore the gate noise. The overall Noise Figure is given by Eq(2).

$$NF = 1 + \frac{\gamma}{\alpha}$$  (2)

Achived Noise figure is approximate 2.2dB. So minimum Noise Figure can be achieved with common gate structure. To acheive Noise Figure less than 2.2dB we consider input resistance with $Z_s$. By considering $Z_s=R_s$, $Z_s=sL_s$, $Z_s=1/sC_s$, lowest noise figure is obtained by $Z_s=sL_s$.

Matching network consists $C_6$, $C_7$ and small inductor. $C_6$ comes because of ESD devices. It could be big as good ESD structure. $C_7$ is because of package PIN.

Fig. 2. LNA Architectures (a) Resistance Match (b) Feedback Structure (c) Common Gate Structure (d) Inductive Degeneration

Rule of thumb says that if you have $I_{bias}=1mA$ than the value of $g_m$ will be 10 times to 20 times the value of $I_{bias}$. For the proposed circuit value of $I_{bias}=3mA$, if device in weak inversion than to fix linearity is very difficult so the device is operating in saturation region. According to thumb rule if the device is biasing at certain current than you should maintain $V_{dsat}$ at 200mV. It means it is strong inversion, if $V_{dsat}$ goes down than $g_m$ goes high for same bias current. The relation between $V_{dsat}$ and $W/L$ is given by equation no (3), and the $c$ is total capacitance which is the sum of the capacitance offered by gate and drain.

$$V_{dsat}^2 = \frac{2I_{bias}}{KNm^2W}$$  (3)

$$C_{gs} = C_{ox} \times w \times l$$  (4)

$$C_{ex} = C_{gs} + 2C_{ds}$$  (5)

$$50\Omega = g_m \times \frac{l_1}{c}$$  (6)

$$f_0 = \frac{1}{2\pi(\frac{f_0}{l_1})C_{ex}}$$  (7)

Value of $c_{gs}$, $c_{ex}$, $L_s$, $f_0$ is calulated by given equations, and the value of gain is given by Eq.(8).

$$gain = \frac{\sqrt{f/c}}{R_2}$$  (8)

$$k = \frac{1+|d|^{-|s11|^2-|s22|^2}}{2|s12||s21|}$$  (9)

$$\Delta = s11s22 - s21s12$$  (10)

$$RL = 10log\frac{P_{out}}{P_{IN}}$$  (11)

$$IL = 10log\frac{P_{out}}{P_{IN}}$$  (12)
TABLE I. DESIGN SPECIFICATIONS

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>180 nm</td>
</tr>
<tr>
<td>Power Supply</td>
<td>1.8 V</td>
</tr>
<tr>
<td>M1</td>
<td>W=200um, L=180nm</td>
</tr>
<tr>
<td>M2</td>
<td>W=200um, L=180nm</td>
</tr>
<tr>
<td>Cds</td>
<td>54fF</td>
</tr>
<tr>
<td>Cgs</td>
<td>264fF</td>
</tr>
<tr>
<td>Cex</td>
<td>372fF</td>
</tr>
<tr>
<td>Ls</td>
<td>266pH</td>
</tr>
<tr>
<td>Lg</td>
<td>1156pH</td>
</tr>
</tbody>
</table>

III. SIMULATION RESULTS AND COMPARISON

The design was stimulated by using 180nm technology. These are the figures (5-8) presents the S parameter curves, from a simulation with the input signal frequency varying from 1 to 10GHz. This figure shows, S11 (input reflection coefficient), S12 (reverse gain coefficient), S21 (forward gain coefficient), S22 (output reflection coefficient) respectively, with the help of S parameter we can calculate insertion, return loss. Insertion loss is calculated by Eq.(12), return loss is calculated by Eq.(11). Figures (9-12) presents Stability Factor, Noise Figure, Compression curve, IIP3. Stability factor is calculated by Eq.(9), for unconditional stability k>1 and Δ<1. The S21 displays a maximum gain of 11.7dB at 1.17GHz. The S12 is -57.16dB, which is less than an excellent value -25.7dB of S12. Table II summarizes the simulated parameters of LNA and compare it with other reported circuit performance.
To provide good noise characteristics, the transistors have been seized while allowing a good input impedance matching over the required frequency. The measured noise figure is shown in Figure 10. Figure 12 shows the simulation result of 1-dB and 3-dB compression point. It can be seen that the value of IIP3 is about -20dBm.

### TABLE II. COMPARISON BETWEEN 2.4GHz CMOS LNAs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[1]</th>
<th>[4]</th>
<th>[6]</th>
<th>[7]</th>
<th>[10]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage(V)</td>
<td>1.2</td>
<td>.8</td>
<td>1.8</td>
<td>.6</td>
<td>1.0</td>
<td>1.8</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>.13um</td>
<td>.13um</td>
<td>.18um</td>
<td>.13um</td>
<td>.18um</td>
<td>.18um</td>
</tr>
<tr>
<td>NF(dB)</td>
<td>4</td>
<td>3.6</td>
<td>2.77</td>
<td>3.8</td>
<td>3.8</td>
<td>.304</td>
</tr>
<tr>
<td>IIP3</td>
<td>-12</td>
<td>-14.3</td>
<td>11.8</td>
<td>-12</td>
<td>-9.1</td>
<td>-20</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.32</td>
<td>.8</td>
<td>18</td>
<td>.12</td>
<td>13</td>
<td>6.5</td>
</tr>
</tbody>
</table>
Table II summarizes the performance of the LNA and compares the other reported circuit performance. Our proposed CMOS LNA achieves low noise figure and power consumption, and compares well with other published report.

IV. CONCLUSION

The LNA proposed in this paper is implemented in 0.18µm CMOS technology. The inductive degeneration topology was chosen for this design as it offers a low noise figure 304dB under 1.8V supply voltage. The transformer used as load in the circuit. The simulation results have shown that the proposed LNA consumes only 6.5mW while achieving a forward gain of 15.72dB, the value of IIP3 is about -20dBm. This LNA has relatively small noise figure and power consumption. It also works in the ISM band.

References